Claims

[c1] What is claimed is:

1.A method of fabricating a stringerless structure on a semiconductor substrate, the method comprising:

forming a first layer on the semiconductor substrate;

forming a spacer on each side wall of the first layer;

forming a second layer to cover the first layer and the spacer, the second layer being thicker than the first layer;

forming a patterned photoresist layer on the second layer;

using the patterned photoresist layer as a mask to perform an anisotropic dry etching process to remove portions of the second layer and the first layer and form a bottom corner stringer beside the spacer;

removing the spacer to expose the bottom corner stringer; and

removing the bottom corner stringer.

[c2] 2.The method of claim 1 wherein the first layer is a patterned gate.

[c3] 3.The method of claim 1 wherein the spacer comprises silicon nitride.

[c4] 4.The method of claim 1 wherein the second layer comprises a silicon oxide layer or a silicon oxide layer containing boron/phosphorous atoms.

[c5] 5.The method of claim 1 wherein a thickness of the spacer ranges from 70 to 120 angstroms (Å) approximately.

[c6] 6.A method of fabricating a stringerless flash memory, the method comprising:

providing a semiconductor substrate, the semiconductor substrate comprising a silicon oxide layer;

forming a plurality of rows of layer stacks on the silicon oxide layer, a shallow trench being formed between two adjacent layer stacks, each layer stack comprising a first polysilicon layer, a sacrificial layer and two side walls;

forming a spacer on each side wall of the layer stacks, the spacer having a predetermined thickness;

depositing a high density plasma (HDP) silicon oxide layer to cover the layer stacks and the shallow trenches;

planarizing the HDP silicon oxide layer to expose the sacrificial layer;

removing the sacrificial layer and a portion of the spacer, such that a remainder of the spacer forms a stringer block;

forming a second polysilicon layer on the first polysilicon layer, the first polysilicon layer combining with the second polysilicon layer to form a floating gate layer;

sequentially forming an insulating layer and a controlling gate layer on the floating gate layer;

performing an anisotropic dry etching process to remove portions of the controlling gate layer, the insulating layer and the floating gate layer, a bottom corner stringer being formed beside the stringer block during the etching process of the floating gate layer;

removing the stringer block to expose the bottom corner stringer; and

removing the bottom corner stringer.

[c7] 7.The method of claim 6 wherein the method further comprises an ion implantation process to form a buried bit line within the semiconductor substrate beneath the shallow trench.

[c8] 8.The method of claim 7 wherein the ion implantation process is performed after the spacer is formed.

[c9] 9.The method of claim 6 wherein a thickness of the spacer ranges from 70 to 120 angstroms (Å) approximately.

[c10] 10.The method of claim 6 wherein a thickness of the stringer block is greater than 50 Å .

[c11] 11.The method of claim 6 wherein a height of the stringer block ranges from 200 to 1000 Å approximately.

[c12] 12.The method of claim 6 wherein the stringer block comprises silicon nitride.

[c13] 13.The method of claim 6 wherein the sacrificial layer comprises silicon nitride.